IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Lawrence T. Clark, et al.	§	Group Art Unit:	
		§		
Serial No.:	10/626,968	§		
		§	Examiner:	
Filed:	July 25, 2003	§		
		§		
For:	Accessing In Parallel Stored Data For Address Translation	§	Atty. Dkt. No.:	ITL.0961US (P16065)
		§		

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

Applicant submits the references listed on the attached form PTO 1449, copies of which are enclosed.

This statement is being filed within three months of the filing date of the application. Please apply any charges or credits to Deposit Account No. 20-1504 (ITL.0961US).

Respectfully submitted,

Date: October 1, 2003

Sanjeev K. Singh under 37 C.F.R. § 10.9(b)
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Date of Deposit: October 1, 2003
I hereby certify under 37 CFR 1.8(a) that this correspondence is being deposited with the United States Postal Service as **first class mail** with sufficient postage on the date indicated above and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Debra Cutrona

INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

ATTY DOCKET NO.	SERIAL NO.
ITL.0961US (P16065)	10/626,968
APPLICANT(S): LAWRENCE T. CLARK ET AL.	
FILING DATE: July 25, 2003	GROUP ART UNIT:

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	A.	US 2001/0000692	05/03/2001	GULIANI ET AL.	365	230.03	
	B.						
	C.						
	D.						
	E.						
	F.						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
	G.							
	H.							
	I.							
	J.							
	K.							

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

	L.	Javier Zalamea, Josep Llosa, Eduard Ayguadé and Mateo Valero; Two-level Hierarchical Register File Organization for VLIW Processors; Department d'Arquitectura de Computadors (UPC) Universitat Politècnica de Catalunya
	M.	Rajeev Balasubramonian, Sandhya Dwarkadas and David H. Albonesi; Department of Computer Science, Department of Electrical and Computer Engineering, University of Rochester; Reducing the Complexity of the Register File in Dynamic Superscalar Processors
	N.	Minda Zhang, Ph.D, Senior software engineer Intel Corporation; Analysis of Object File Formats for Embedded Systems; June, 1995; pages 1-22
	O.	Steven Wallace and Nader Bagherzadeh; Department of Electrical and Computer Engineering, University of California, Irvine, CA; A Scalable Register File Architecture for Dynamically Scheduled Processors; Published in the Proceedings of the International Conference on Parallel Architectures and Compilation Techniques '96, October 21-23, 1996 in Boston, Massachusetts
	P.	Toni Juan (Dept. of Computer Architecture, Univ. Politècnica de Catalunya, Barcelona, Spain), Tomas Lang (Dept. of Electrical and Computer Engineering, Univ. California Irvine) and Juan J. Navarro (Dept. of Computer Architecture, Univ. Politècnica de Catalunya, Barcelona, Spain); Reducing TLB Power Requirements; 1997; pages 196-201
	Q.	
	R.	

EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.